CLAIMS

WHAT IS CLAIMED IS:

1. A method for decoding data blocks, comprising:

demodulating a first data transmission transmitted via a first modulation scheme to obtain a first sequence of bits, the first sequence of bits representing a first data block comprising a first payload;

detecting an error associated with the first data block;

storing the first sequence of bits;

demodulating a second data transmission transmitted via a second modulation scheme to obtain a second sequence of bits, the second sequence of bits representing a second data block comprising a second payload, the second payload comprising at least a portion of the first payload;

combining a portion of the first sequence of bits with a portion of the second sequence of bits to obtain a third sequence of bits;

appending an other portion of the first sequence of bits to the third sequence of bits to obtain a fourth sequence of bits; and

decoding the fourth sequence of bits to obtain the first data block.

2. The method of claim 1, wherein the first and second data blocks are punctured before being transmitted, the method further comprising:

depuncturing the first sequence of bits; and

depuncturing the second sequence of bits;

wherein the combining a portion of the first sequence of bits with a portion of the second sequence of bits comprises:

adding portions of the depunctured second sequence of bits to corresponding portions of the depunctured first sequence of bits.

3. The method of claim 1, further comprising:

determining whether an error exists with regard to the fourth sequence of bits.

4. The method of claim 1, wherein the portion of the first sequence of bits comprises higher protocol layer information and a portion of the first payload and the other portion of the first sequence of bits comprises an other portion of the first payload.

5. The method of claim 4, wherein the portion of the second sequence of bits corresponds to higher protocol layer information and the second payload; and

wherein the combining a portion of the first sequence of bits with a portion of the second sequence of bits comprises:

adding the portion of the first sequence of bits with a corresponding portion of the second sequence of bits.

6. The method of claim 1, further comprising:

determining whether the fourth sequence of bits contains an error; and

decoding the third sequence of bits to obtain the second data block, when the fourth sequence of bits contains an error.

7. The method of claim 6, further comprising:

detecting an error in the second data block; and

combining the third sequence of bits with an other portion of the second sequence of bits to obtain a fifth sequence of bits, the other portion of the second sequence of bits corresponding to an error check field and higher protocol layer information.

8. The method of claim 1, further comprising:

detecting an error in the fourth sequence of bits;

demodulating a third data transmission transmitted via the second modulation scheme to obtain a fifth sequence of bits, the fifth sequence of bits representing a third data block comprising a third payload, the third payload comprising a portion of the first payload;

combining a portion of the first sequence of bits with a portion of the fifth sequence of bits to obtain a sixth sequence of bits;

appending an other portion of the first sequence of bits to the sixth sequence of bits to obtain a seventh sequence of bits; and

decoding the seventh sequence of bits to obtain the first data block.

9. The method of claim 8, further comprising:

determining whether the seventh sequence of bits contains an error; and

decoding the sixth sequence of bits to obtain the third data block, when the seventh sequence of bits contains an error.

10. The method of claim 1, further comprising:

determining whether an error exists in the four sequence of bits;

decoding the third sequence of bits to obtain the second data block, when an error exists in the fourth sequence of bits;

demodulating a third data transmission transmitted via the second modulation scheme to obtain a fifth sequence of bits, the fifth sequence of bits representing a third data block comprising a third payload, the third payload comprising a portion of the first payload;

combining a portion of the first sequence of bits with a portion of the fifth sequence of bits to obtain a sixth sequence of bits;

decoding the sixth sequence of bits to obtain the third data block; and

appending a sequence of bits representing the second payload to a sequence of bits representing the third payload when no error exists in either the second or third data blocks, the appended second and third payloads corresponding to the first payload.

11. A device for decoding data blocks, comprising:

a receiver that receives data transmissions;

a demodulator coupled to the receiver, the demodulator:

demodulating a first data transmission transmitted via a first modulation scheme to obtain a first sequence of bits, the first sequence of bits representing a first data block comprising a first payload, and

demodulating, after the first data transmission, a second data transmission transmitted via a second modulation scheme to obtain a second sequence of bits, the second sequence of bits representing a second data block comprising a second payload, the second payload comprising a portion of the first payload;

an error detector that determines whether an error exists in the first data block;

a memory that stores the first sequence of bits when an error in the first data block is detected;

a combiner that combines a portion of the first sequence of bits with a portion of the second sequence of bits to obtain a third sequence of bits and appends an other portion of the first sequence of bits to the third sequence of bits to obtain a fourth sequence of bits; and

a decoder that decodes the fourth sequence of bits to obtain the first data block.

12. The device of claim 11, wherein the first and second data blocks are punctured before being transmitted, the device further comprising:

a depuncturing circuit that:

depunctures the first sequence of bits, and

depunctures the second sequence of bits;

wherein when combining, the combiner adds portions of the depunctured second sequence of bits with corresponding portions of the depunctured first sequence of bits.

13. The device of claim 11, wherein the error detector further determines whether an error exists in the fourth sequence of bits.

14. The device of claim 11, wherein the portion of the first sequence of bits corresponds to higher protocol layer information and a portion of the first payload and the other portion of the first sequence of bits comprises an other portion of the first payload.

15. The device of claim 14, wherein the portion of the second sequence of bits corresponds to higher protocol layer information and the second payload, wherein when combining, the combiner adds the portion of the first sequence of bits with a corresponding portion of the second sequence of bits.

16. The device of claim 11, wherein the decoder further:

decodes the third sequence of bits to obtain the second data block, when the fourth sequence of bits contains an error.

17. The device of claim 16, wherein the combiner:

combines the third sequence of bits with an other portion of the second sequence of bits to obtain a fifth sequence of bits, when the second data block contains an error, the other portion of the sequence of bits corresponding to an error check field and higher protocol layer information.

18. The device of claim 11, wherein when the error detector determines that an error exists in the fourth sequence of bits:

the demodulator demodulates a third data transmission transmitted via the second modulation scheme to obtain a fifth sequence of bits, the fifth sequence of bits representing a

third data block comprising a third payload, the third payload comprising a portion of the first payload,

the combiner combines a portion of the first sequence of bits with a portion of the fifth sequence of bits to obtain a sixth sequence of bits and appends an other portion of the first sequence of bits to the sixth sequence of bits to obtain a seventh sequence of bits, and

the decoder decodes the seventh sequence of bits to obtain the first data block.

19. The device of claim 18, wherein the error detector further determines whether an error exists in either seventh sequence of bits, and

the decoder decodes the sixth sequence of bits to obtain the third data block, when the seventh sequence of bits contains an error.

20. The device of claim 11, wherein when the error detector determines that an error exists in the fourth sequence of bits:

the decoder decodes the third sequence of bits to obtain the second data block,

the demodulator demodulates a third data transmission transmitted via the second modulation scheme to obtain a fifth sequence of bits, the fifth sequence of bits representing a third data block comprising a third payload, the third payload comprising a portion of the first payload,

the combiner combines a portion of the first sequence of bits with a portion of the fifth sequence of bits to obtain a sixth sequence of bits,

the decoder decodes the sixth sequence of bits to obtain the third data block, and

the combiner appends a sequence of bits representing the second payload to a sequence of bits representing the third payload when no error exists in either the second or third data blocks, the appended second and third payloads corresponding to the first payload.

21. A computer-readable medium having stored thereon a plurality of sequences of instructions, said instructions comprising sequences of instructions which, when executed by at least one processor, cause said processor to:

demodulate a first data transmission transmitted via a first modulation scheme to obtain a first sequence of bits, the first sequence of bits representing a first data block comprising a first payload;

detect an error associated with the first data block;

store the first sequence of bits;

demodulate a second data transmission transmitted via a second modulation scheme to obtain a second sequence of bits, the second sequence of bits representing a second data block comprising a second payload, the second payload comprising a portion of the first payload;

combine a portion of the first sequence of bits with a portion of the second sequence of bits to obtain a third sequence of bits;

append an other portion of the first sequence of bits to the third sequence of bits to obtain a fourth sequence of bits; and

decode the fourth sequence of bits to obtain the first data block.

22. The computer-readable medium of claim 21, further comprising instructions for causing said processor to:

detect an error in the fourth sequence of bits;

demodulate a third data transmission transmitted via the second modulation scheme to obtain a fifth sequence of bits, the fifth sequence of bits representing a third data block comprising a third payload, the third payload comprising a portion of the first payload;

combine a portion of the first sequence of bits with a portion of the fifth sequence of bits to obtain a sixth sequence of bits;

append an other portion of the first sequence of bits to the sixth sequence of bits to obtain a seventh sequence of bits; and

decode the seventh sequence of bits to obtain the first data block.

23. The computer-readable medium of claim 21, further comprising instructions for causing said processor to:

detect whether an error exists in the fourth sequence of bits;

decode the third sequence of bits to obtain the second data block, when the fourth sequence of bits contains an error.

demodulate a third data transmission transmitted via the second modulation scheme to obtain a fifth sequence of bits, the fifth sequence of bits representing a third data block comprising a third payload, the third payload comprising a portion of the first payload;

combine a portion of the first sequence of bits with a portion of the fifth sequence of bits to obtain a sixth sequence of bits;

decode the sixth sequence of bits to obtain the third data block; and

append a portion of the bits in the second data block representing the second payload to a portion of the bits in the third data block representing the third payload, the appended second and third payloads corresponding to the first payload.

24. A method for decoding data blocks, comprising:

demodulating a first data block transmitted via a first modulation scheme to obtain a first set of soft bits associated with the first data block;

detecting an error in the first data block;

transmitting a negative acknowledgement message to a transmitting device;

storing the first set of soft bits;

demodulating a second data block transmitted via a second modulation scheme to obtain a second set of soft bits associated with the second data block;

identifying the second data block as being part of a split data block;

combining a portion of the first set of soft bits with a portion of the second set of soft bits to obtain a first sequence of bits;

appending an other portion of the first set of soft bits to the first sequence of bits to obtain a second sequence of bits; and

decoding the second sequence of bits to obtain the first data block.

25. The method of claim 24, wherein the first and second data blocks are transmitted according to enhanced data rates for global system for mobile communications and time division multiple access evolution (EDGE) protocol, the portion of the first set of soft bits correspond to an F field, an E field and a portion of a payload of the first data block, the portion of the second set of soft bits correspond to an F field, an E field and a payload of the second data block and the other portion of the first set of soft bits correspond to the remaining portion of the payload of the first data block, a cyclic redundancy check field and a tail field.

26. The method of claim 24, further comprising:

determining whether an error exists in the second sequence of bits; and

decoding the first sequence of bits to obtain the second data block when an error exists in the second sequence of bits.

27. The method of claim 24, further comprising:

detecting an error in the second sequence of bits;

demodulating a third data block transmitted via the second modulation scheme to obtain a third set of soft bits;

identifying the third data block as part of the split data block;

combining a portion of the first set of stored soft bits with a portion of the third set of soft bits to obtain a third sequence of bits; and

appending an other portion of the first set of soft bits to the third sequence of bits to obtain a fourth sequence of bits; and

decoding the fourth sequence of bits to obtain the first data block.

28. The method of claim 27, wherein the combining a portion of the first set of stored soft bits with a portion of the third set of soft bits to obtain a third sequence of bits comprises:

omitting a predetermined number of bits in the combining to obtain the third sequence of bits, the predetermined number of bits relating to a memory of an encoder used to encode the first and third data blocks.

29. The method of claim 28, wherein the predetermined number of bits include bits corresponding to a first portion of a second half of a payload field of the first data block.

30. The method of claim 29, wherein the predetermined number of bits include bits corresponding to an F field and an E field and a first portion of a payload field of the third data block.

31. A device for decoding data blocks, comprising:

a memory for storing soft bits generated by demodulating data blocks; and

a receiver that:

demodulates a first data block transmitted via a first modulation scheme,

transmits a negative acknowledgement message to a transmitting device, when an error is detected in the first data block,

demodulates a second data block transmitted via a second modulation scheme,

identifies the second data block as being part of a split data block,

combines a portion of the soft bits associated with the first data block with a portion of the soft bits associated with the second data block to obtain a first sequence of bits,

appends an other portion of the soft bits associated with the first data

block to the first sequence of bits to obtain a second sequence of bits, and

decodes the second sequence of bits to obtain the first data block.

32. The device of claim 31, wherein the receiver:

detects an error in the second sequence of bits, and

decodes the first sequence of bits to obtain the second data block when an error exists in the second sequence of bits.

33. The device of claim 31, wherein the receiver:

detects an error in the second sequence of bits,

demodulates a third data block transmitted via the second modulation scheme,

identifies the third data block as being part of the split data block,

combines a portion of the soft bits associated with the first data block with a portion of the soft bits associated with the third data block to obtain a third sequence of bits,

appends an other portion of the first set of soft bits to the third sequence of bits to obtain a fourth sequence of bits, and

decodes the fourth sequence of bits to obtain the first data block.

34. The device of claim 33, wherein the receiver:

detects an error in the first data block,

decodes the first sequence of bits to obtain the second data block,

decodes the third sequence of bits to obtain the third data block, and

appends a sequence of bits representing a payload of the second data block with a sequence of bits representing a payload of third data block, the appended bits representing a payload of the first data block.

35. A mobile terminal, comprising:

a memory that stores data bits generated by demodulating data blocks; and

a receiver that:

demodulates a first data block comprising a first payload, the first data block transmitted via an eight phase shift keying (8PSK) modulation scheme,

detects an error in the first data block,

stores a first set of bits associated with the first data block in the memory,

transmits a negative acknowledgement message to a transmitting device that transmitted the first data block, when an error is detected,

demodulates a second data block transmitted via a Gaussian minimum shift keying (GMSK) modulation scheme to obtain a second set of bits, the second data block comprising a second payload comprising a portion of the first payload,

combines a portion of the second set of bits with a portion of the first set of bits to obtain a first sequence of bits,

appends an other portion of the first set of bits to the first sequence of bits to obtain a second sequence of bits, and

decodes the second sequence of bits to obtain the first data block.

36. The mobile terminal of claim 35, wherein the receiver further:

demodulates a third data block transmitted via a GMSK modulation scheme to obtain a third set of bits, the third data block having a third payload comprising a second half of the first payload,

combines a portion of the third set of bits with a portion of the first set of bits to obtain a third sequence of bits,

appends an other portion of the first set of bits to the third sequence of bits to obtain a fourth sequence of bits, and

decodes the fourth sequence of bits to obtain the first data block.

37. A method for decoding a plurality of data blocks, each of the plurality of data blocks comprising a portion of a payload of a first data block transmitted via a first modulation scheme, the method comprising:

demodulating the plurality of data blocks, the plurality of data blocks transmitted via a second modulation scheme;

combining a portion of stored data bits associated with the first data block with one of a plurality of sequences of bits generated by demodulating one of the plurality of data blocks;

appending the remaining portion of the stored data bits to the results of the combining; and

decoding the results of the appending to obtain the first data block.

38. The method of claim 37, further comprising:

detecting an error in the first data block;

decoding the plurality of data blocks using at least a portion of the stored data bits associated with first data block; and

appending a portion of the decoded bits associated with each of the plurality of data blocks, the appended bits representing the payload of the first data block.

39. A method for decoding a plurality of data blocks, each of the plurality of data blocks comprising a portion of a payload of a first data block transmitted via a first modulation scheme, the method comprising:

demodulating a first data block transmitted via a first modulation scheme to obtain a first set of soft bits;

demodulating second and third data blocks transmitted via a second modulation scheme to obtain a second and third set of soft bits, respectively;

combining a portion of the first set of soft bits with a portion of each of the second set and third set of soft bits, respectively, to obtain a first sequence of bits; and

performing a bi-directional decoding on the first sequence of bits to obtain the first data block.

40. The method of claim 39, wherein the performing a bi-directional decoding on the first sequence of bits to obtain the first data block comprises:

performing a first decoding operation beginning at a first end of the first sequence of bits, the first end representing a beginning of the first data block; and

performing a second decoding operation beginning at a second end of the first sequence of bits, the second end presenting a tail portion of the first data block.

41. The method of claim 40, further comprising:

determining whether either one of the first and second decoding operations results in no errors, wherein a sequence of bits generated by an error free decoding represents the first data block.

42. A device for decoding data blocks, comprising:

a memory that stores first probability information associated with a demodulated first data block;

a MAP decoder that:

receives an input bit sequence corresponding to a second data block, the first and second data blocks being transmitted via different modulation schemes and the second data block comprising a portion of the first data block, and

outputs second probability information associated with the second data block using the first probability information; and

a processing device that converts the output from the MAP decoder to a binary sequence of bits representing the first data block.

43. The device of claim 42, wherein the MAP decoder:

receives an input bit sequence corresponding to a third data block, the second and third data blocks being transmitted via a same modulation scheme and the third data block comprising a portion of the first data block, and

outputs third probability information associated with the third data block using the first probability information, and

the processing device:

converts the output from the MAP decoder to a binary sequence of bits representing the first data block, and

determines whether an error exists in the first data block.

44. A method for decoding data blocks, comprising:

demodulating a first data block transmitted via a first modulation scheme to obtain a first set of soft bits associated with the first data block, the first data block having a first payload;

detecting an error in the first data block;

storing the first set of soft bits;

demodulating a second data block and a third data block transmitted via a second modulation scheme to obtain a second and a third set of soft bits associated with the second and third data blocks, respectively, the second and third data blocks each comprising a portion of the first payload;

combining a portion of the first set of soft bits with a portion of the second set of soft bits to obtain a fourth set of soft bits;

decoding the fourth set of soft bits to a point corresponding to the beginning of the third data block;

calculating output bits at the point corresponding to the beginning of the third data block for each of a number of surviving states relating to the memory of an encoder that encoded the first data block;

comparing the calculated output bits to output bits generated when the starting state of the encoder for the third data block is known;

modifying the third set of soft bits based on the comparison;

combining the modified third set of soft bits to at least one of a portion of the first or fourth set of the soft bits associated with the second half of the first payload to obtain a fifth set of soft bits; and

decoding the fifth set of soft bits.

45. The method of claim 44, wherein the result of decoding the fourth set of soft bits comprises a first half of the first payload and the result of decoding the fifth set of soft bits comprises a second half of the first payload, the method further comprising:

appending bits representing the first half of the first payload to bits representing the second half of the first payload, the appended bits representing the first payload.